Open Meeting About US ATLAS Liquid Argon (LAr) Calorimeter Phase II Upgrade Planning

John Parsons
Columbia University

July 13, 2015
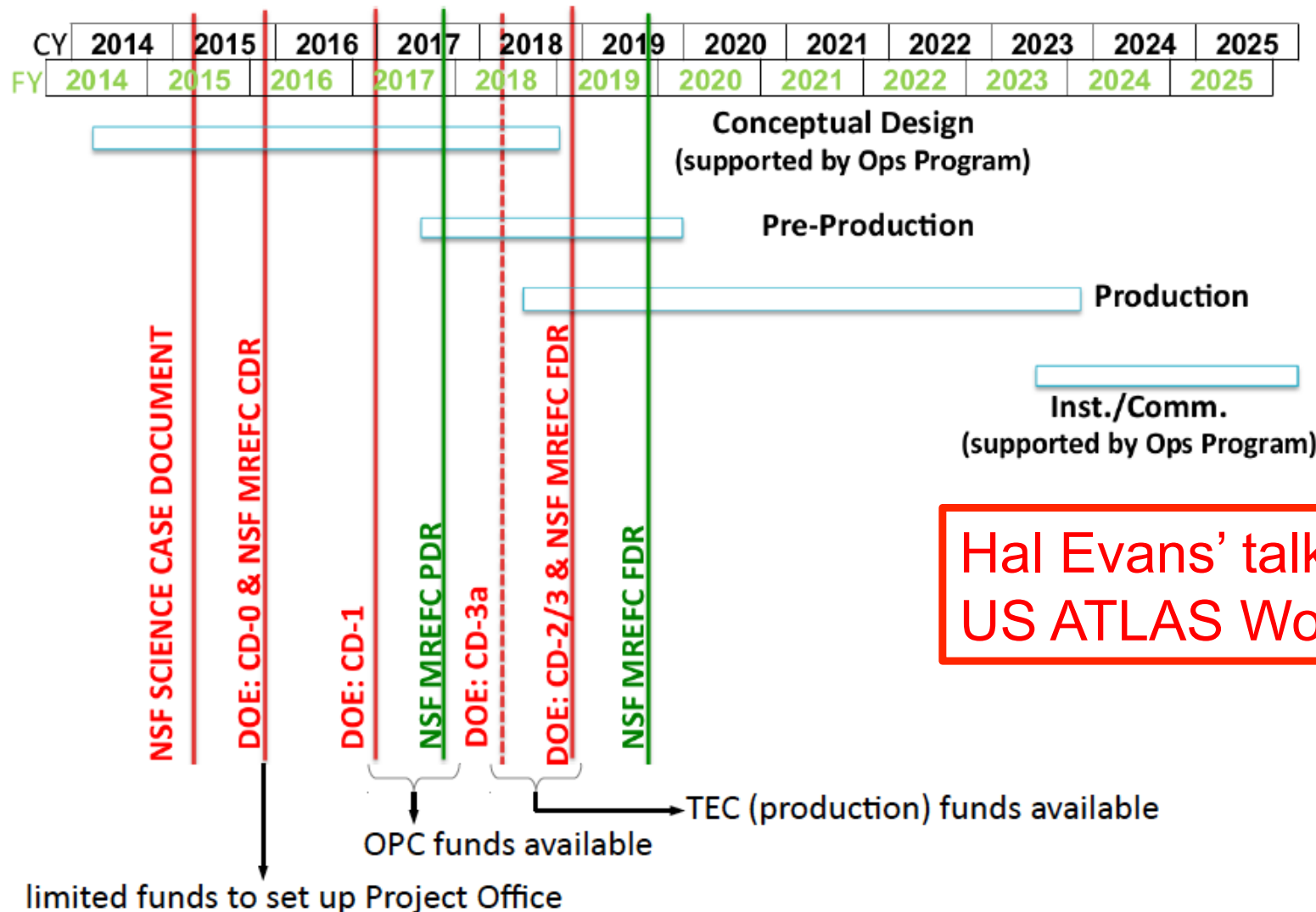
LAr Phase-II Organization

❖ Modest US R&D funding supporting sFCAL effort as well as ASIC design for frontend electronics

❖ JP appointed in Jan. as LAr Phase II construction manager

❖ US ATLAS working toward preparing DoE and NSF proposals for Phase II construction project

  ▪ Need to define scope, institutional responsibilities, cost and manpower, …

  ▪ Draft WBS, planning etc. being worked on

6.3 LAr: WBS DICTIONARY

WBS	Name	Institute
6.3.1	**FCAL**	
6.3.1.1	**FCAL Mechanics**	
6.3.1.1.1	FCAL Mechanics Arizona	Arizona
6.3.1.1.2	FCAL Mechanics Iowa	Iowa
6.3.1.2	**FCAL Cold Electronics**	**Arizona**
6.3.2	**Frontend Electronics**	
6.3.2.1	**Preamp/shaper**	
6.3.2.1.1	Preamp/shaper BNL	BNL
6.3.2.1.2	Preamp/shaper UPenn	UPenn
6.3.2.2	**ADC/Gain Selector**	
6.3.2.2.1	ADC/Gain Selector Nevis	Nevis
6.3.2.2.2	ADC/Gain Selector UTD	UTDallas
6.3.2.3	**Optical links**	
6.3.2.3.1	ADC/Link Interface	
6.3.2.3.1.1	ADC/Link Interface Nevis	Nevis
6.3.2.3.1.2	ADC/Link Interface SMU	SMU
6.3.2.3.2	Electrical components	SMU
6.3.2.3.2	Optical components	SMU
6.3.2.4	**FEB2 System Integration**	
6.3.2.4.1	FEB2 System Integration Nevis	Nevis
6.3.2.4.2	FEB2 System Integration BNL	BNL
6.3.2.5	**FEB2 PCB**	**Nevis**
6.3.2.6	**Radiation qualification and testing**	
6.3.2.6.1	Radiation qualification and testing BNL	BNL
6.3.2.6.2	Radiation qualification and testing Nevis	Nevis
6.3.2.6.3	Radiation qualification and testing UPenn	UPenn
6.3.2.6.4	Radiation qualification and testing SMU	SMU
6.3.2.6.5	Radiation qualification and testing UTAustin	UTAustin
6.3.3	**Backend Electronics**	
6.3.3.1	**Firmware and software**	
6.3.3.1.1	Firmware and software Arizona	Arizona
6.3.3.1.2	Firmware and software BNL	BNL
6.3.3.1.3	Firmware and software MSU	MSU
6.3.3.1.4	Firmware and software Oregon	Oregon
6.3.3.1.5	Firmware and software StonyBrook	StonyBrook
6.3.3.2	**Hardware**	

LAr Phase II Upgrade Project

• Readout Electronics

LAr hadronic end-cap (HEC)

LAr electromagnetic end-cap (EMEC)

LAr electromagnetic barrel

• LAr FCAL
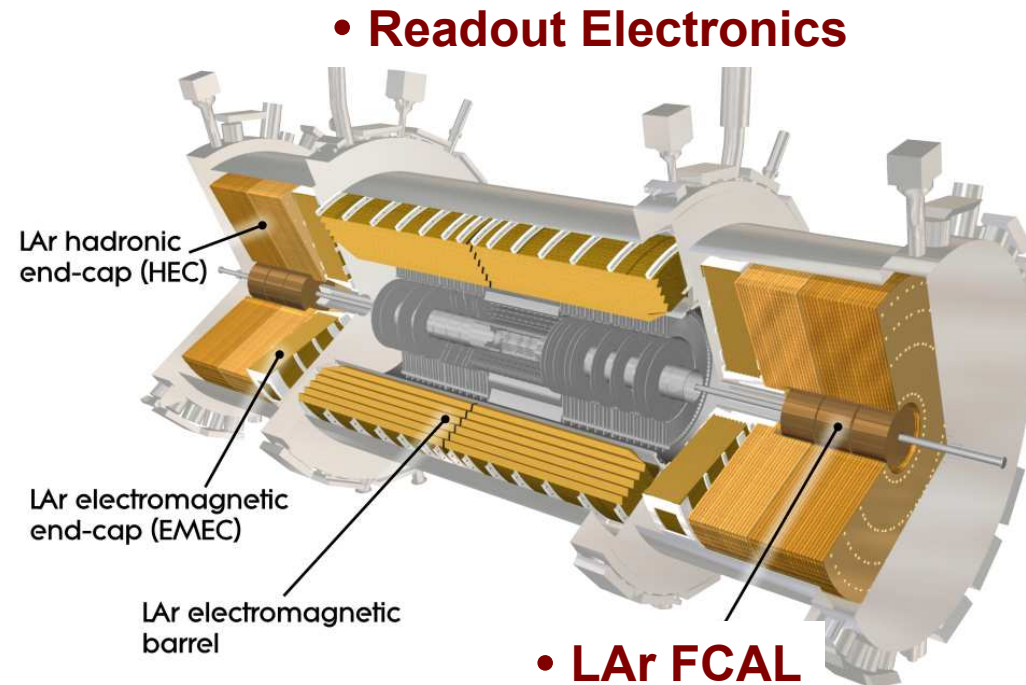
ATLAS LAr Phase II Upgrade:
• Replace the LAr readout electronics
• Modify the forward region, including:
      • possible new (s)FCAL   (or miniFCAL)
   • possible new forward precision timing detector

FCAL

LAr Detector Options in LoI

- Option 0: No change neither of the HEC cold electronics nor of the FCal detectors.

- ~~Option 1: If the HEC cold electronics have to be replaced (Sec. 3.2.2), the large cold cryostat cover would have to be opened and the irradiated FCal would have to be removed. A newly built cold FCal (sFCal) (Sec. 3.2.3) would then be inserted before closing the cryostat.~~

- Option 2: If the HEC cold electronics do not have to be replaced, the cold FCal would be replaced by a new one of the sFCal type (Sec. 3.2.3). It is anticipated that only the small cover of the cold vessel, the FCal bulkhead, would have to be removed.

- Option 3: If the HEC cold electronics do not have to be replaced, the cold FCal would stay in place and a new small calorimeter (Mini-FCal) (Sec. 3.2.4) would be placed in front of it. In this case only the cryostat warm vessel would have to be opened.

Endcap Cryostat

- **HEC cold electronics do not need to be replaced, so there is no need to remove the large cold cover (means FCAL summing boards not accessible)**
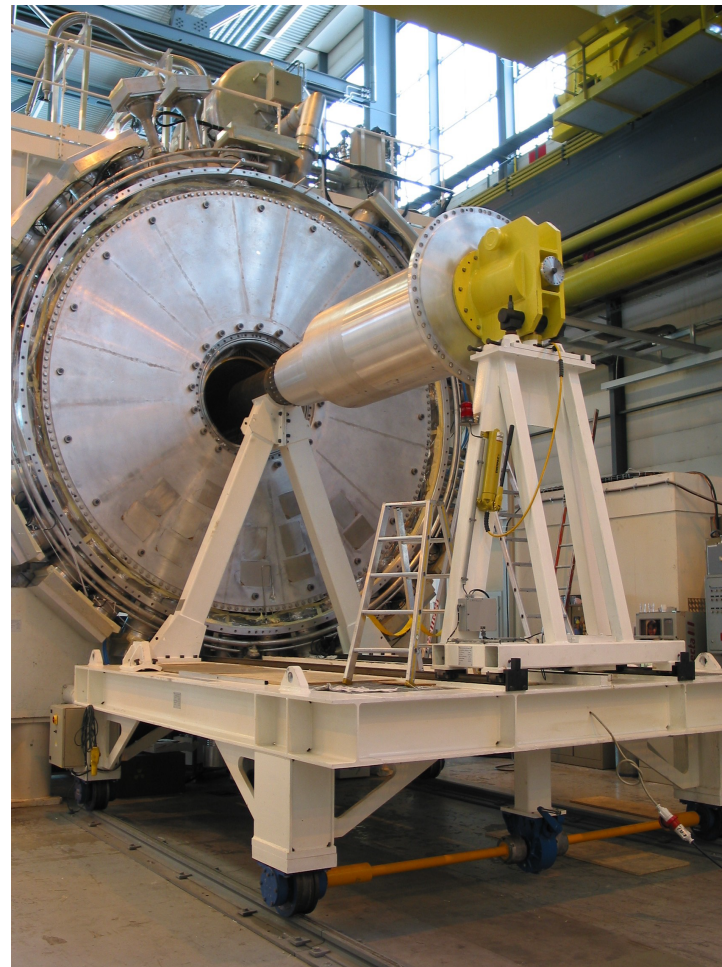
Forward Calorimeter

❖ ATLAS EM and hadronic calorimeter detectors are able to cope with HL-LHC conditions

❖ Only exception is ATLAS FCAL, which uses novel (US) design with absorber rods housed in absorber lattice, and small LAr gaps (270 – 500 μm)

❖ Beyond design luminosity, enormous rates lead to space charge problems (even possibly boiling of LAr), as well as voltage drops across HV resistors

- Utilizing the same design concept but with thinner gaps (down to 100 μm), one could tolerate the HL-LHC conditions

- Using this technique, solutions being investigated include:
  o A new calorimeter ("sFCAL"), or
  o A "Mini-FCAL"
  (placed in front of the existing FCAL)
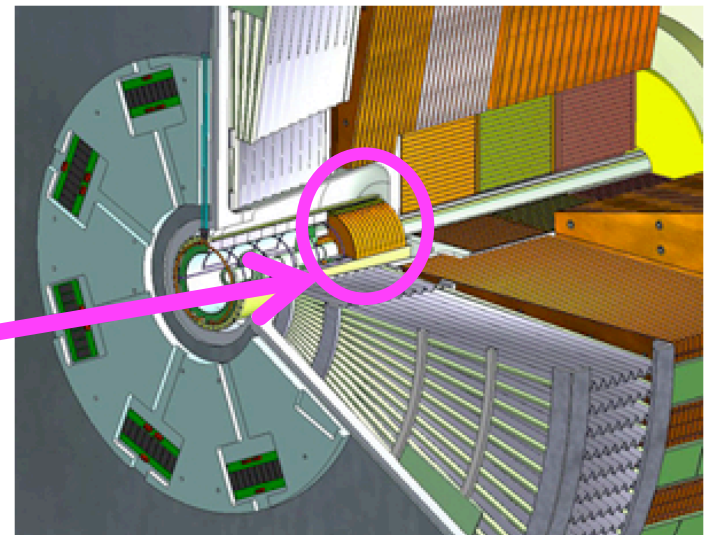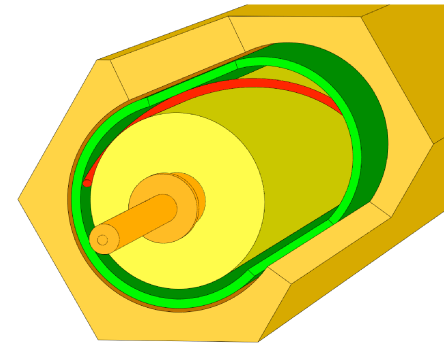
FCAL (cont'd)

❖ Recent simulations suggest LAr will not boil (though margin is small)

- However, geometry is complicated and difficult to simulate accurately
- A mockup has been built, but testing is so far inconclusive
- Further LAr sub-cooling by ΔT= -1.6 K successfully tested during recent shutdown (and ΔT= -2 K is believed to be possible)

❖ FCAL performance issues have been discussed by large-eta task force (LETF)

- Gets tied in with fwd tracking, possible new timing and/or "preshower-type" detector in space previously occupied by MBTS, etc. (see later)
- Suggestion has also been made to increase readout granularity in case of sFCAL (probably only in EM-compartment, sFCAL1)
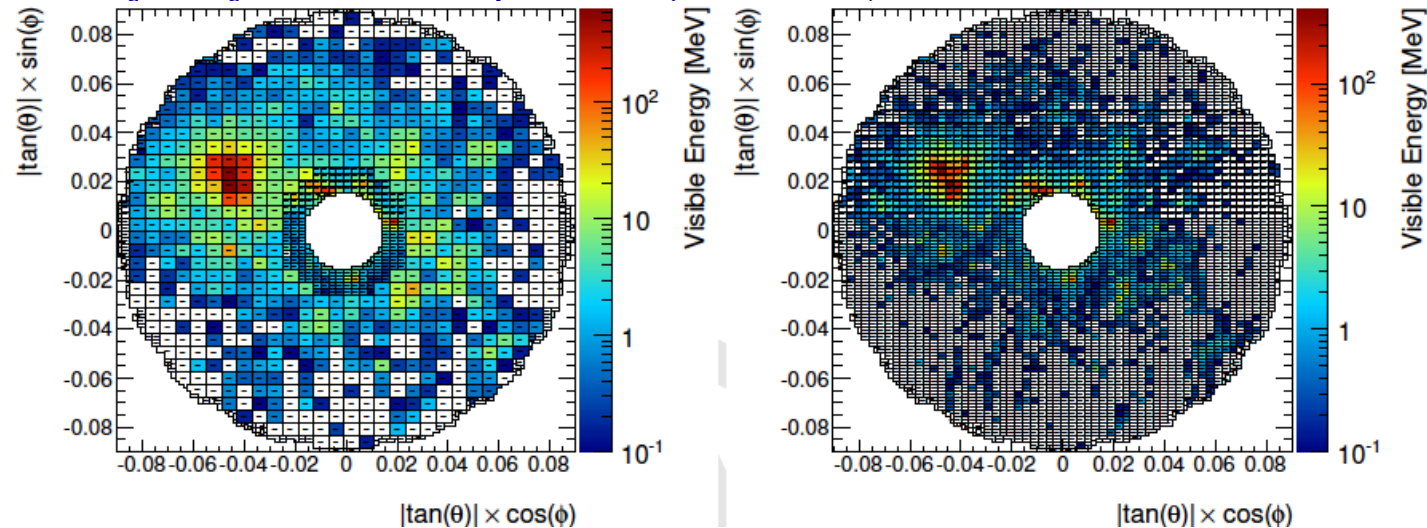
FCAL Decision

❖ **Decision of final approach still to be made**

  ▪ Originally scheduled for March 2015

  ▪ Pushed back, with review now scheduled for December 2015 (any later could jeopardize readiness of sFCAL for when it is needed for installation)

  ▪ Continuing to work on multiple fronts, to prepare decision:

    ○ Finalize understanding of whether LAr boiling will occur if no change is made in the forward region

    ○ Explore performance, and associated physics impact, of various scenarios (degraded FCAL, sFCAL with low/high granularity, miniFCAL)

      – VERY limited (physicist) manpower available

    ○ Work to solve engineering issues related to realization of miniFCAL concept

❖ **Until final decision, need to carry options**

Readout Electronics

New LAr Readout Electronics

❖ To adapt to Phase II TDAQ architecture, need to replace LAr readout

- Current readout would continue to limit L1 rate to 100 kHz, and latency to ~ 2.5 μs

❖ Plan to develop new "FEB2", digitizing and sending off detector all channels at 40 MHz

- Move pipeline off detector, out of radiation environment

- Have full granularity calo. info available for new L1 trigger, so that shower shape info, etc. can be used to allow EM trigger thresholds to remain low

- Use Phase I LAr trigger upgrade electronics as part of new L0 trigger used to seed Phase II L1 track trigger

❖ Will also need new backend electronics to receive and process the FEB2 data (boundaries between LAr and TDAQ become more blurry, certainly for L1)

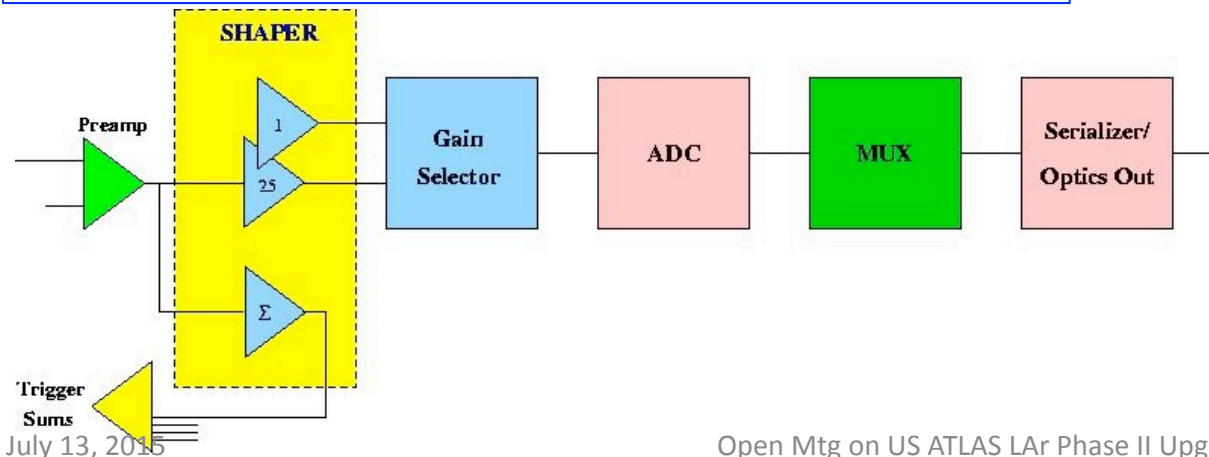**Red for Phase I. Blue for Phase II.**

The front-end:
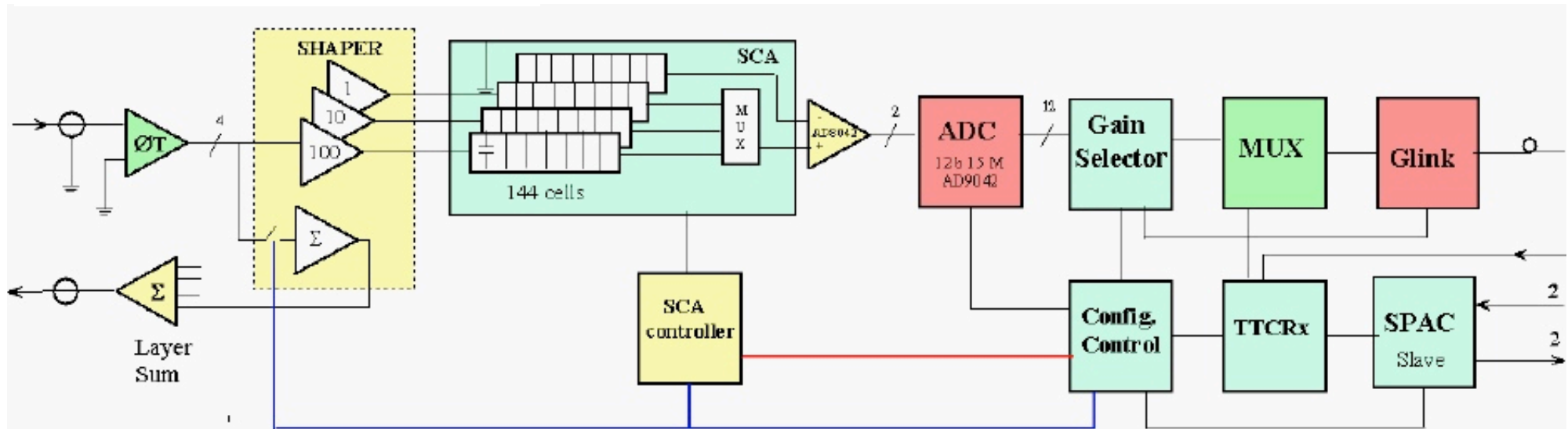
Current detector readout scheme on the (US-designed) FEB

Proposed readout upgrade (FEB2)

Critical R&D:
1. Pre-amp + Shaper
2. ADC (12 to 16 bit)
3. Optical Link (10 G)

July 13, 2015

LAr FE Electronics Developments

❖ Main goal of current R&D is the investigation of the potential of 65 nm CMOS to meet the various needs for FEB2 ASICs:

- Preamp/shaper ASIC

  o Prototyped originally in SiGe (UPenn/BNL)

  o New BNL effort on 65 nm CMOS, with major challenge being 16-bit dynamic range

  o By fall, Upenn will shift focus to help with 65 nm investigation

- ADC

  o 130 nm ADC (pipeline + SAR) developed at Columbia is nearing production phase for use in Phase I, and design effort has turned to 65 nm for Phase II

  o Formed new collaboration with UT Dallas, who is focusing (on all-SAR version) in 65 nm

- Optical links

  o Need ~100 Gpbs of rad-tol optical link bandwidth per 128-channel FEB2

  o SMU working on serializer/driver for ~ 10 Gbps optical link, as well as optical components (as part of Versatile Link project)

❖ In ~1 year, should have enough experience (and even first prototypes) to gauge potential to use 65 nm as a common technology for the various blocks

  o Later step would see whether further ASIC consolidation would be possible/desirable

LAr BE Electronics

❖ Readout of FEB2 will require new backend electronics

❖ Full granularity data will be used for both precision readout (eg. in offline analysis) as well as for triggering at L1 and above

  ▪ Boundaries between LAr and TDAQ subsystems become more blurry

❖ A lot to be learned from the Phase I LAr trigger upgrade, where the LDPS will receive and process data from "super-cells" at 40 MHz

❖ BE construction responsibilities for Phase II are so far less advanced than for FE

  ▪ Current RODs were built by European collaborators, and considerable interest exists there for a similar role in Phase II

  ▪ In any case, US groups are playing significant roles in Phase I LDPS, and will bring this expertise to planning of BE electronics for Phase II

Possible High-Granularity Timing Detector (HGTD)

HGTD

❖ Scoping Document includes possible new "4D" detector in space of current MTBS

■ Δz = 60 mm detector could cover η of 2.4 – 4.1 (5.0)

❖ Aiming for time res'n of 30-50 ps and spatial granularity of 1-100 mm^2

❖ Possibly multiple layers, if also used as preshower

❖ Synergy with possible Si/Cu miniFCAL (and also CMS)

❖ More MC studies needed to optimize design and evaluate ability to use timing to reject pileup, select PV, …
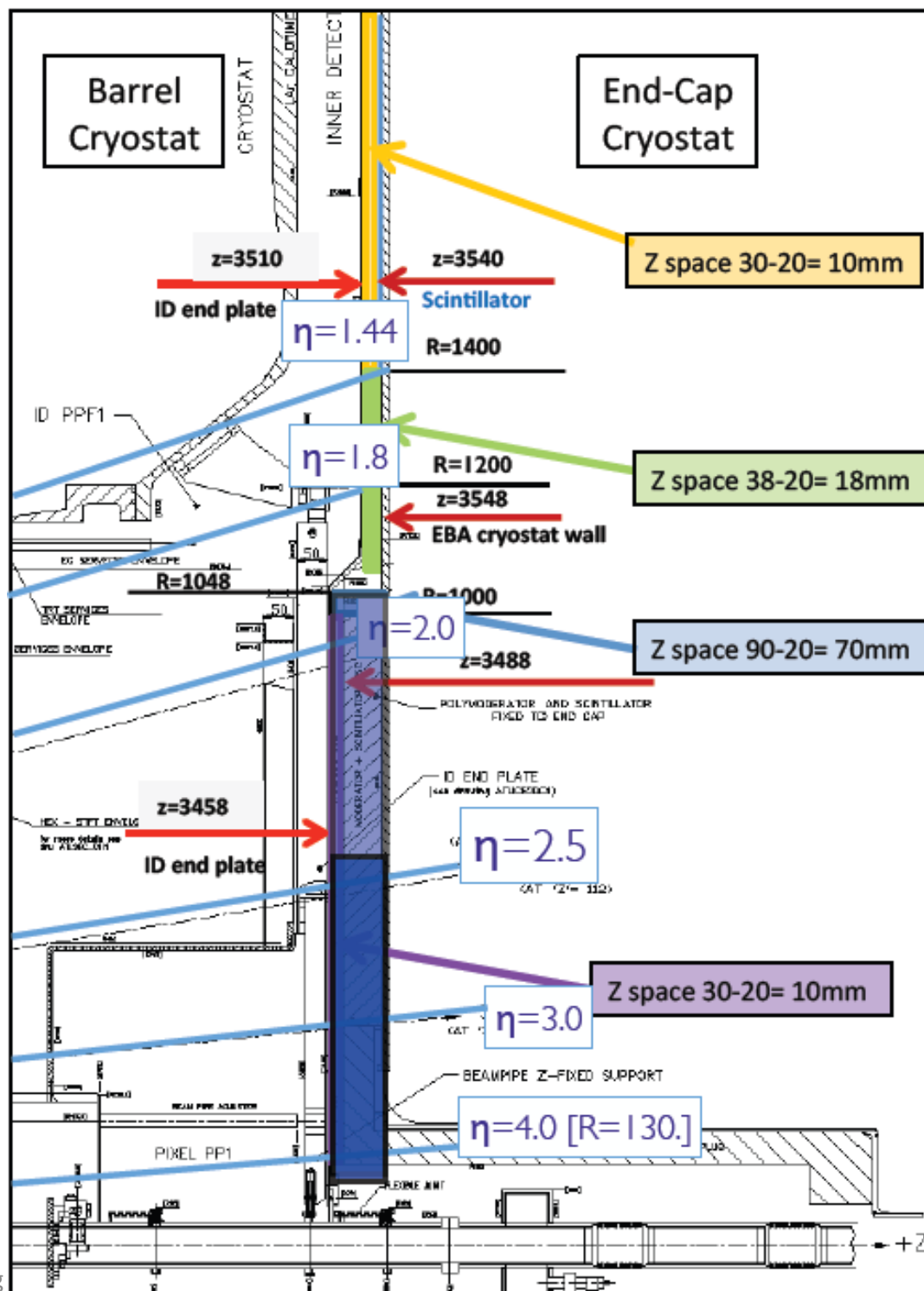
Timing Detector Organization

❖ First mtg was held on July 3/2015

https://indico.cern.ch/event/403701/

❖ Abe Seiden presented ideas about using ultra-fast Si detectors

❖ Known US interests so far include UCSC, Oregon, BNL

❖ ATLAS has scheduled ~monthly mtgs to organize this new effort

US LAr Institutions

❖ **sFCAL (or MiniFCAL)**
- U Arizona
- Interest from U Iowa

❖ **Frontend Electronics Components**
- BNL, Columbia, U Penn, SMU, UT Dallas
- Interest from UT Austin

❖ **FEB2 and Frontend System Integration FEB2**
- BNL, Columbia

❖ **Backend Electronics**
- U Arizona, U Oregon, Stony Brook, BNL
- Interest from MSU

❖ **Timing Detector**
- Interest from UCSC, Oregon, BNL

Summary (Part I)

❖ US ATLAS is playing many critical roles in ongoing LAr Phase II planning

❖ FCAL upgrade option will be finalized around end of 2015. US plans to contribute in either sFCAL or miniFCAL scenarios

❖ Readout upgrade concentrates on FEB2 and US is leading the efforts. Current R&D centered on FE components and options that will influence the system integration. Decisions in the R&D course will guide the efforts to construction.

❖ There is also considerable US interest and expertise in the BE electronics. Discussions concerning BE responsibilities are less advanced so far (and will involve also TDAQ/LAr boundaries).

❖ A new issue is a possible HGTD, in which a few US institutes have already expressed interest.

Summary (Part II)

❖ To prepare for DoE and NSF construction proposals (and corresponding CD-0 and CDR reviews), need to make rapid progress on scope, institutional responsibilities, costs, manpower, ...

❖ Any new institutes who are interested in participating should contact JP as soon as possible

❖ Proposals for technical contributions should be accompanied by scientific (ie. physicist) commitments

   ▪ A great way to get started is to join the urgent simulation effort that is required (and VERY under-staffed) to evaluate the physics case for the upgrade, to optimize the designs, and to choose among the various options

Backup Slides

Process for Developing Scope

❖ **U.S. Scope (deliverables) expressed in a WBS + Budget/Schedule**

- being developed by L2 Managers

WBS	System	L2 Manager	WBS	System	L2 Manager
6.1	Pixels	P. Grenier (SLAC)	6.2	Strips	C. Haber (LBNL)
6.3	LAr	J. Parsons (Columbia)	6.4	TileCal	M. Oreglia (Chicago)
6.5	Muons	T. Schwarz (Michigan)	6.6	TDAQ	E. Lipeles (Penn), J. Zhang (ANL)

- driven by expertise developed in the U.S. (reflected in R&D program)
- current status summarized on next slides

Hal Evans' talk at US ATLAS Workshop

❖ **Timeline for WBS/Budget/Schedule**

- Aug/Sep 2015: scrubbing of sub-system WBS/Budget/Schedule
- Oct 2015: snapshot "frozen" for CD-0/CDR
- 2016-18: further scope development for CD-1,2/3 / PDR/FDR
  - note that scope changes become more difficult with time
- end 2018: scope is fixed after CD-2/3 / FDR

Table 12. Numbers of electrodes, interconnects and readout channels for the ATLAS FCal. For the high-granularity sFCal, the number of readout channels could be increased to the number of interconnects by removing a signal summing stage that is currently done on board in the cold volume of the endcap cryostat.

	Electrodes	Interconnects	Channels
FCal1	12,260	3066	1008
FCal2	10,200	1700	500
FCal3	8,224	914	254
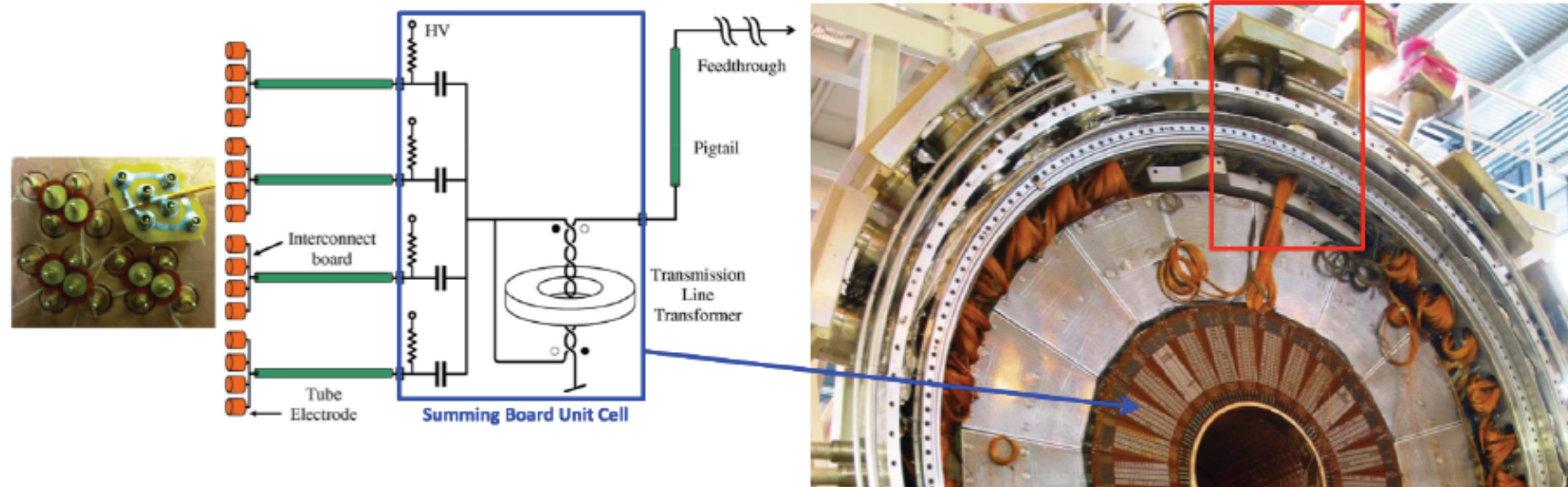
Figure 24. This figure illustrates the summing of signals for the FCal1. On the left is a schematic of how the signals from four groups of electrodes are summed on boards located on the rear face of the HEC (seen on the right). Also visible on the right (highlighted) is the FCal signal feed-through serving the half-crate that is currently used for the FCal front-end electronics. The HV distribution is also performed on the summing boards, which carry the current-limiting protection resistors referred to in the text.

Installation time schedule

Green light for side A	0 days	
Green light for side C	0 days	
Side A	100.75 days	
Install minivans + FCAL extension tube + rotary table + shielding	1.5 days	
Move cryostat to Z 13000 (horizontal tilt as an option)	1 day	
Measure radiation levels	0.5 days	
Remove JM Shielding (+ Scintillator 7)	5.5 days	
Extract warm cover and inner warm tube	8.5 days	
Extract FCal structure	21.5 days	
Fcal feedthrough modification	16.5 days	
Insert new FCal structure + new LVDT system	15.5 days	
Weld leak tightness bands on seals	20 days	
Mount warm cover and insert inner warm tube (Final)	13.5 days	
Preparation for closing	9 days	
Ready for closing operations	0 days	
ECA Calorimeter ready	0 days	
Purge cold vessel	2 wks	
Cool-down	9 wks	
Fill (Ar condensation, including GHe/ Gar exchange)	10 days	
Side C	120.5 days	
Install minivans + FCAL extension tube + rotary table + shielding	1.5 days	
Move cryostat to Z 13000 (horizontal tilt as an option)	1 day	
Measure radiation levels	0.5 days	
Remove JM Shielding (+ Scintillator 7)	5.5 days	
Extract warm cover and inner warm tube	8.5 days	
Extract FCal structure	39 days	
Fcal feedthrough modification	15 days	
Insert new FCal structure + new LVDT system	15.5 days	
Weld leak tightness bands on seals	20 days	
Mount warm cover and insert inner warm tube (Final)	13.5 days	
Preparation for closing	9 days	
Ready for closing operations	0 days	
ECC Calorimeter ready	0 days	
Purge cold vessel	2 wks	
Cool-down	9 wks	
Fill (Ar condensation, including GHe/ Gar exchange)	2 wks	

Side A : 20 weeks
+ 12 weeks for cooling

Side C starts week #13

Side C completed on week #36
+ 12 weeks for cooling

M. Raymond

LAr phase II Engineering – March 04th, 2015

5

sFCal Production schedule

Main milestones of the last sFCal production schedule (Sept. 2012)

sFCal R&D : Sept. 2011 – Feb. 2014
sFCal approval : Beginning 2015
sFCal1 production : Jan. 2015 → Apr. 2020
sFCal2 production : Nov. 2015 → Feb. 2020
sFCal3 production : Jan. 2016 → Oct. 2019

Will High Granularity sFCal need more production time ?

sFCal-A integration (at Cern) : Jan. 2018 → March 2020
sFCal-A beam calibration : May 2020 → Aug. 2020

sFCal-C integration (at Cern) : Jul. 2019 → May 2021
sFCal-C beam calibration : May 2021 → Aug.2021

Some optimization is possible here for contingencies

Preparation for installation : Sept. 2021 → Dec. 2021

sFCal ready for installation in the cryostat (both) : Beg. 2022

Providing the production can really start just after the approval, a decision by end of 2015 is still consistent with a status "ready for installation" by beg. 2023
but very close to be critical
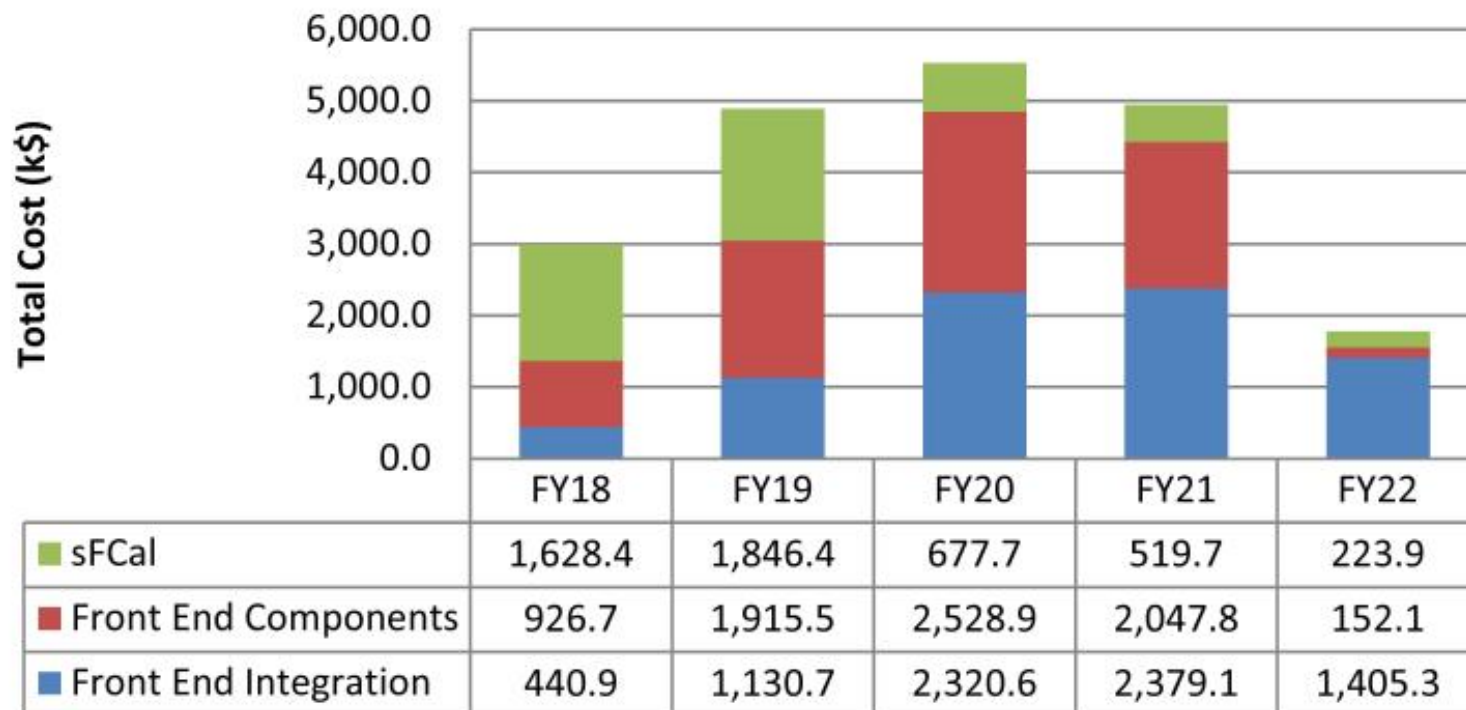
FE System-on-Chip

The idea has been around awhile but now it's a proposal
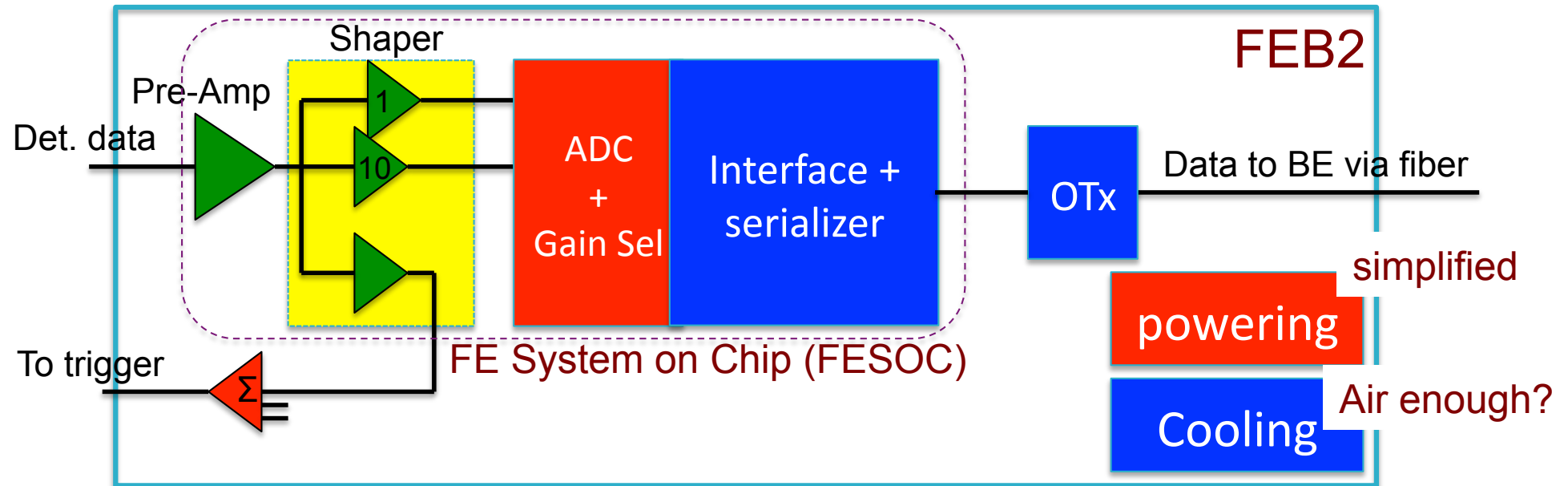
- FESOC, a one die or two die chip that integrates the three key ASICs. By combining the ADC with the serializer (both in 65 nm CMOS), one eliminates the output circuits for the ADC hence saves power.
- Impact on system integration and in construction:
  - Simplified FEB2, powering and possibly air (not water) cooling.
  - Reduce production cost in chip packaging and QA, and in FEB PCB.
  - The impact on yield may be small as the yield of 65 nm CMOS is expected to be high and the cost of die is small.
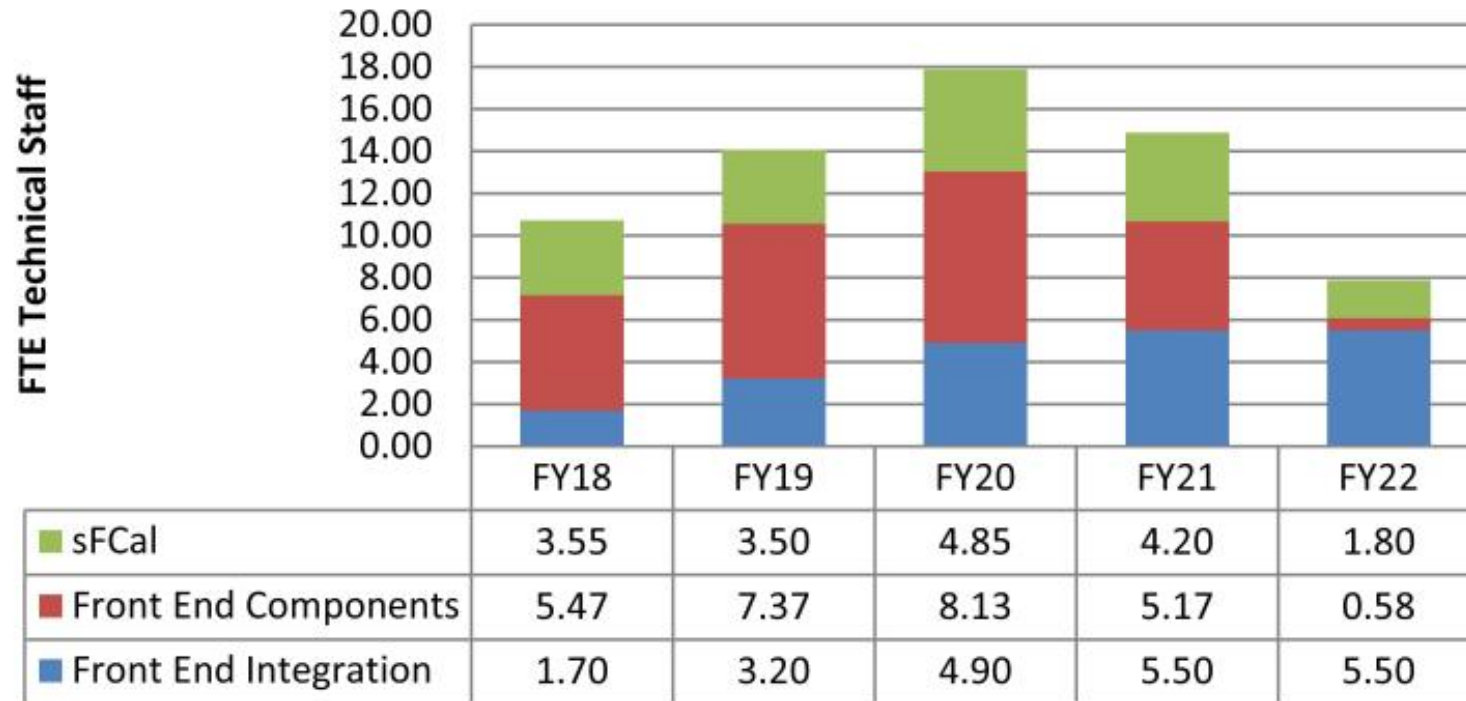
US LAr Phase 2 Construction Total Cost

Total Cost (k$)	FY18	FY19	FY20	FY21	FY22
sFCal	1,628.4	1,846.4	677.7	519.7	223.9
Front End Components	926.7	1,915.5	2,528.9	2,047.8	152.1
Front End Integration	440.9	1,130.7	2,320.6	2,379.1	1,405.3

Item	Cost (k$)
sFCal	4,896
Front End Components	7,571
Front End Integration	7,677
Total	20,144

US LAr Phase 2 FTE Technical Staff

	FY18	FY19	FY20	FY21	FY22
sFCal	3.55	3.50	4.85	4.20	1.80
Front End Components	5.47	7.37	8.13	5.17	0.58
Front End Integration	1.70	3.20	4.90	5.50	5.50

Item	Tech FTE
sFCal	17.9
Front End Components	26.7
Front End Integration	20.8
Total	65.4